RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

ADELL DVA ADELL ADELL SEDD ASDD	R-x	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPEN RX9 SREN CREN ADDEN FERR OERR	RX9D	OERR	FERR	ADDEN	CREN	SREN	RX9	SPEN

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The size of this register is also 8 bits. The role of each bit is discussed below:

SPEN: Serial Port Enable bit

1 =Serial port enabled (configures pin RC7/RX/DT for receiving the information into the PIC, and pin RC6/TX/CK for transmitting the information from PIC)

0 = Serial port disabled

RX9: 9th -bit Receive Enable bit

1 = enables reception of 9 bit

0 = enables reception of 8 bit

SREN - Single Receive Enable bit - this bit enables or cancels transmission of packets. In the asynchronous mode - this bit is not important. The importance of this bit is only in the synchronous mode (Half-Duplex) and only when PIC is Master.

Asynchronous mode:

Don't care.

Synchronous mode - Master:

1 = Enables single receive

0 = Disables single receive

This bit is cleared after reception is complete.

Synchronous mode - Slave:

Don't care.

CREN - Continuous Receive Enable bit

Asynchronous mode:

1 = Enables continuous receive

0 = Disables continuous receive

Synchronous mode:

1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)

0 = Disables continuous receive

ADDEN - Address Detect Enable bit - this bit enables interrupt only when the frame size is 9-bit. It does not matter, when the size of the frame is 8-bit.

Asynchronous mode 9-bit (RX9 = 1):

1 =Enables address detection, enables interrupt and load of the receive buffer when RSR[8] is set

0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit

FERR - Framing Error bit

Logic level "1" – means the STOP bit was not received. In serial communication we use START bit and STOP bit when transmitting the information.

1 = Framing error (can be updated by reading RCREG register and receive next valid byte)

0 = No framing error

OERR - Overrun Error bit

Logical level "1" means that new byte of data was received, while there is still previous data that did not proceed into the PIC. In this case, the new received information is lost.

1 = Overrun error (can be cleared by clearing bit CREN)

0 = No overrun error

RX9D: 9th bit of Received Data, in the case of receiving 9-bits.