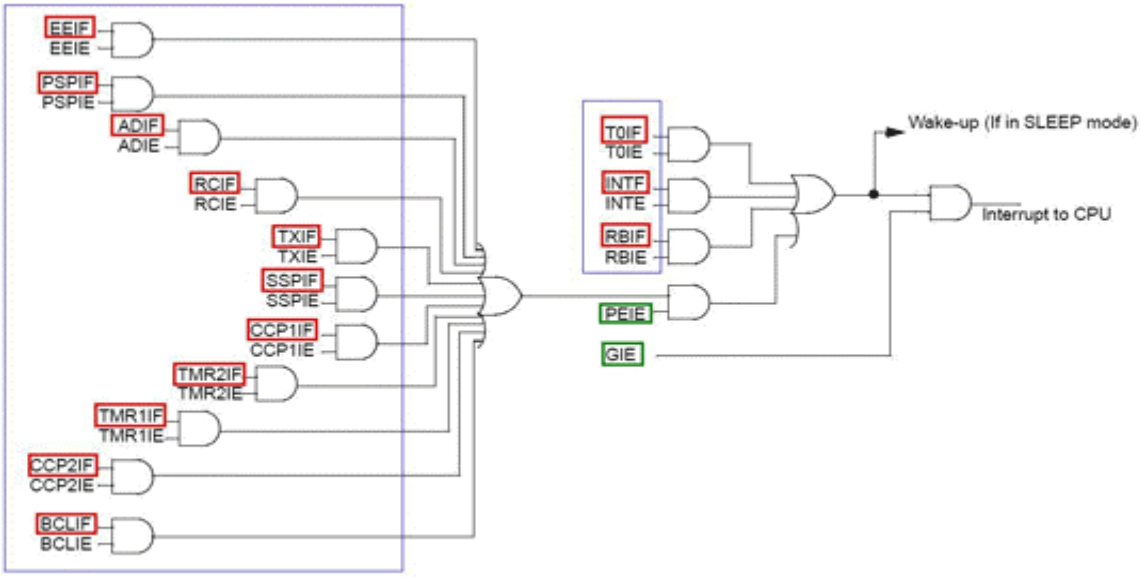
Let's introduce the existing interrupts (in the order they are appearing in figure):



1. *EEIF - EEPROM Write Operation Interrupt Flag bit*
This flag bit appears in the memory components such Data EEPROM and Flash Program Memory located inside the PIC. The interrupt flag EEIF is used to show that the writing process to the memory is completed. In order to write to the memory again, the EEIF must be cleared in the software.

2. *PSPIF – Parallel Slave Port Read/Write Interrupt Flag bit*
This interrupt flag appears when we are utilizing PORTD. PORTD operates as an 8-bit wide Parallel Slave Port (PSP), or microprocessor port, when control bit PSPMODE (TRISE<4>) is set. Interrupt flag PSPIF is designed to inform that the operation of reading/writing from/to PORTD is ended.

3. *ADIF - A/D Converter Interrupt Flag bit*
This interrupt flag associated with A/D component (converting information from analog to digital). A/D Converter Interrupt Flag bit is set when the A/D conversion completed and the result has already saved in the register ADRESH: ADRESL. The flag is intended to flag processor, that the A/D converter is free and can start making a new conversion.

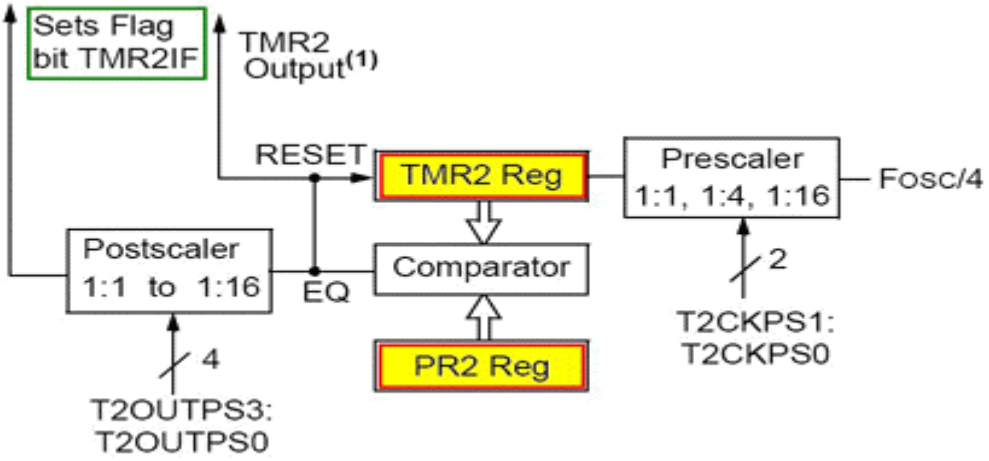
4. *RCIF - USART Receive Interrupt Flag bit*
This interrupt flag appears in the USART unit when it is used as a receiver. The flag RCIF marks an action of receiving the information. When the information that was sent, reached the receiver, it's saved first at the shift RSR register. Immediately after that, the information is moved to RCREG register.
After the information is moved to RCREG register, the USART Receive Interrupt Flag bit - RCIF is set (RCIF=1); This flag let's processor know that RCREG register is full and can not receive more information; the new information will overwrite the existing information that is stored inside the RCREG register.
The flag is cleared by the hardware automatically, as soon as the information stored inside the RCREG register is moved into the PIC microcontroller and the register is empty. This marks that processor can receive a new information.

5. *TXIF - USART Transmit Interrupt Flag bit*
This interrupt flag appears in the USART unit when it is used as a transmitter. The flag marks that the transmitter is ready to receive new information for transmission. The information/data we want to transmit is stored in the temporary register TXREG, where the information/data "waits" to be moved to the register TSR, from where it will be transmitted. When the register TXREG is empty,the USART Transmit Interrupt Flag bit is set (TXIF = 1). This flag let's processor know that a new/additional information/data can be uploaded to the TXREG register for the transmission. As long as TXREG register contains information/data – the TXIF flag will be zero (TXIF=0), to mark that the USART transmit buffer is full.

6. *SSPIF - Synchronous Serial Port (SSP) Interrupt Flag bit*
This interrupt flag appears in the Master Synchronous Serial Port (MSSP) module, which is a serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc.

7. *CCP1IF - CCP1 Interrupt Flag bit*
This interrupt flag appears in the Capture / Compare Module.

8. *TMR2IF - TMR2 to PR2 Match Interrupt Flag bit*
This interrupt flag appears in the TIMER2 module. This module can be used as a counter or as frequency divider, depends on the values of TMR2 and PR2 registers. Register TMR2 contains the initial value for the counting, and register PR2 contains the final value for the counting. When the value of the register TMR2 is equal to the value of the register PR2, the flag TMR2IF is set to indicate the end of counting. You can see how the unit operates in the following figure:



9. *TMR1IF - TMR1 Overflow Interrupt Flag bit*
This interrupt flag appears within timer module TIMER1. Timer1 can operate in one of two modes:
• as a timer
• as a counter
The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h and starts the counting again. The TMR1 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit, TMR1IE (PIE1<0>).

10. ***CCP2IF - CCP2 Interrupt Flag bit***
This interrupt flag appears in the Capture / Compare Module

11. ***BCLIF - Bus Collision Interrupt Flag bit***
This interrupt flag appears in MSSP. The Master Synchronous Serial Port (MSSP) module is a serial interface, useful for communicating with other peripheral or microcontroller devices.

12. ***T0IF***
This interrupt flag appears in timer/counter module TIMER0. The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit TMR0IF (INTCON<2>). Bit TMR0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt.

13. ***INTF - RB0/INT External Interrupt Flag bit***
This is universal external interrupt flag bit. The external interrupt can appear through the pin RB0 of PORTB, when PORTB set as an input.

14. ***RBIF - RB Port Change Interrupt Flag bit***
This flag is set if at least one of the RB7:RB4 pins changed state. In order to enable this interrupt, pins RB7: RB4 must be defined as input.